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CDIO IMPLEMENTATION IN ENGINEERING MODULE IN COVID SCENARIOS

Abstract:

This paper describes the CDIO (CDIO Standard 3.0) implementation in 2nd year cross diploma core module Microcontroller Application (MAPP) at the School of Electrical and Electronic Engineering (School of EEE), Singapore Polytechnic (SP) in COVID (Coronavirus Disease) scenarios. It focuses on the revised Design-Implement Experiences (in CDIO standard 5) and adjusted Engineering Learning Workspaces (in CDIO standard 6) in the module due to the COVID pandemic. The students grasped a common or minimum acceptable level of not only theory knowledge, but also practical skills, which adequately prepared them for the module CDIO project. It shows that students were able to make a rapid adaptation and transition from normal classes to online learning spaces and time-compressed face to face design – implement experience. The revised Design-Implement Experiences and adjusted Engineering Learning Workspaces presented in this paper is a practice of adapting CDIO in engineering education in a scenario with abrupt change.

Keywords:

Microcontroller, Engineering education, CDIO

JEL Classification: I20

Introduction

MAPP was created by then module coordinator with CDIO implementation in mind more than 10 years ago (C. Ping, C. Chiang, C. Teoh, P. Chow, 2010) in School of EEE, Singapore Polytechnic. It is a 6 credit Unit (CU) module taken by all 2nd year students of all diplomas in EEE, Singapore Polytechnic, with around 400 students in total per semester. Table 1 below is the MAPP module's typical practical teaching schedule in a non COVID-hit semester.

Table 1: Practical teaching schedule for MAPP in non COVID-hit semester

Term	Teaching Week	Practical Hrs Per Week	CDIO Stage	Remarks
1	1	**4**	1 hr C	CDIO project briefing, students forming project team
1	2	**4**	1 hr C	**C**onceive
1	3	**4**	1 hr C	**C**onceive
1	4	**4**	1 hr C / D	**C**onceive / **D**esign
1	5	**4**	1 hr D	**D**esign
1	6	**4**	1 hr D	**D**esign
1	7	**4**	1 hr C / D	Presenting the **C**onceived idea with initial **D**esign
Team Break				
2	8	**4**	2 hr I	Project **I**mplementation starts
2	9	**4**	2 hr I	**I**mplementation
2	10	**4**	4 hr I	**I**mplementation
2	11	**4**	4 hr I	**I**mplementation
2	12	**4**	4 hr I	**I**mplementation
2	13	**4**	4 hr I	**I**mplementation
2	14	**4**	4 hr I / O	**O**perating the projects with implementation completed
2	15	**4**	4 hr O	**O**perating the rest projects.

Source: MAPP module teaching and learning plan

Notes: The word "module" in Singapore Polytechnic is equivalent to "subject" in universities.

Before the COVID pandemic, MAPP was implemented in flipped teaching with one hour lecture content in the format of byte sized video developed by the module specialist, which students were required to complete this part of learning via Self Directed Learning (SDL) before practical lesson started; the other hour-long mass lecture was conducted face to face in campus lecture theatre by teaching staff. The C - D - I - O stage activity was carried out in campus lab face to face weekly.

Table 2 below lists the assessment components of the MAPP module. There is no change for the assessment components and their weightages before and during COVID.

Table 2. Assessment components of MAPP module

Assessment Components	Weightage
General Performance	10%
Lab Test	15%
Project (Conceive / Design)	15%
Mid Semester Test	20%
Project (Implement with Demo)	30%
Supervised Online Quizzes	10%

Source: MAPP module

The COVID pandemic in Singapore started in Mar 2020. Staff were informed that term one of new semester starting in mid-April 2020 until the June term break, there would be no face to face lessons on campus. Instead, all the lessons were to be moved to online.

Hence, there was a need to revise Design-Implement Experiences and adjust Engineering Learning Workspaces to make sure students were adequately trained and ready to move onto the next stage of learning.

Revised Design-Implement Experiences and Adjusted Engineering Learning Workspaces

As mentioned in the previous section, the COVID broke out in March 2020 before the Academic Year 2020 / 2021 Semester One (AY2021S1) started. Since week 1 of term 1 AY2021 until June term break, all the lessons, including practical lessons were conducted online. The online practical lesson was in e-practical format with circuit design and code explanation, emulation and pre-recorded practical demo by lecturer via team collaboration software, e.g. Microsoft Teams, Skype, Zoom, etc., followed by SDL e-practical by students.

Project (Conceive / Design) assessment was conducted online via presentation of student group project proposal with defined problem statement and student group conceived solution using microcontroller, including system block diagram design, circuit design, software flowchart design, etc.

Mid Semester Test was conducted in COVID Mid-Semester Test (cMST) format, a unique remotely supervised online assessment format to ensure both academic integrity and rigor of the assessment upheld (T. Khoon, C. Leong, T. Joo, S. Anwar, 2021).

Supervised Online Quizzes consists of 8 topic quizzes. Similarly, term 1 Supervised Online Quizzes were conducted in COVID Formative Assessment (cFA) format, a unique remotely supervised online assessment format to ensure both academic integrity and rigor of the assessment upheld (T. Khoon, C. Leong, T. Joo, S. Anwar, 2021).

The Lab Test was postponed to term 2 with the hope of face to face assessment to be allowed on campus, which turned out to be true, with the improved Covid situation in Singapore in 2020.

In AY2021 S1 Term 2 which started end-June 2020, half of the class's students were allowed to return to campus for face to face hands-on activities and ensure there was sufficient space between every two students so that face to face learning on campus is safe in COVID scenario. Term 2 Supervised Online Quizzes and Project (Implementation, Operation with Demo) Assessment were conducted in two batches per class face to face on campus, with half of the class in each batch at most.

Throughout AY2021 S2 which started mid-October 2020, when the COVID scenario further improved in Singapore, half of the class's students were allowed to carry out hand-on activities on campus. All the assessments were carried out face to face on campus as before COVID pandemic, but in two batches, except for MST which was conducted in one setting with full class fact to face on campus.

Table 3 below shows the revised Design-Implement Experiences and Adjusted Engineering Learning Workspaces during the COVID pandemic, compared to those in normal semesters.

Table 3. Comparison of practical lesson before and during COVID pandemic

Comparison / Lesson	Normal Terms (Non-COVID Hit Semester)	AY2021 S1 Term 1 (COVID Hit Semester)	AY2021 S1 Term 2 and AY2021 S2 (COVID Hit Semester)
4 hour Practical	**Full class** face to face **on campus**: • 3-hour **face to face hands-on practical** in Lab venue supervised by lecturer. Plus, • 1 hour hands-on practical unsupervised, on CDIO project, assisted by Technical Executives (TE). working on Lab activities, including coding on microcontroller to interface with I / O devices, circuit design, working on CDIO project.	**Full class online**: • Synchronous 1.5 hour **e-practical** delivered by lecturer, using practical guide in e-bound notes, and **simulation** software. Plus, • 2.5-hour **e-practical** by students via SDL using byte-sized **Lab video**, working on Lan activity and C - D of the CDIO project	**Half class** face to face **on campus**, half class e-learning at home: • **Bi-weekly** 3 hour **face to face combined hands-on practicals** in the Lab with **half class students** for Labs and CDIO project, supervised by lecturer. Plus, • **Bi-weekly** 1 hour unsupervised **hands-on practical** with the same **half of the class face to face** in the Lab by students using byte-sized **Lab video** on CDIO project, assisted by TEs. The rest half of students carried out e-practical via SDL at home bi-weekly, using byte-sized **Lab video** on Lab activities and CDIO project

Source: MAPP module teaching and learning plan

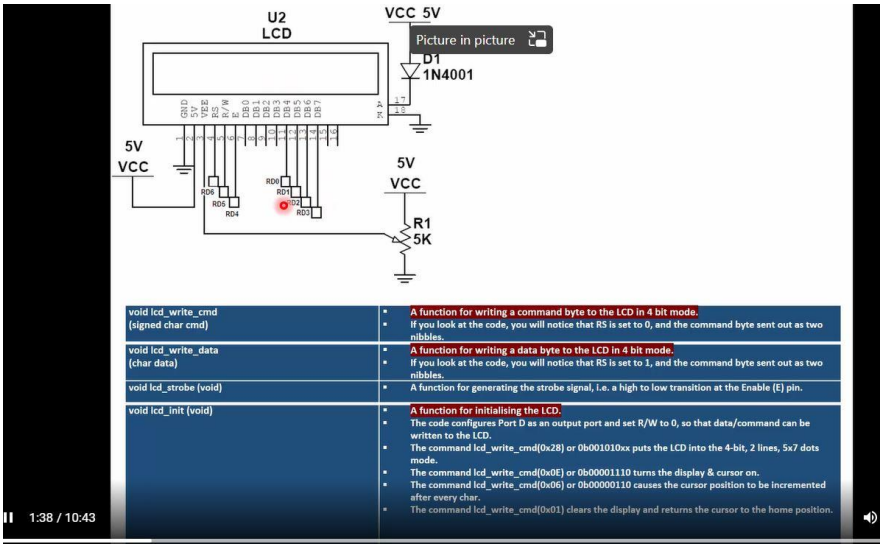
During Jun term break of AY2021 S1, compressed catch-up hands-on practicals for term 1 were conducted in two batches with half of the class in each batch face to face in the campus lab. The synchronous e-practical with lecturer and self directed e-practical by students in term 1, in addition to the compressed catch-up hands-on on campus during term break, well prepared MAPP module students for achieving a common or minimum acceptable level of module practical skills. This could be seen in the 86.8% AY2021 S1 passing rate for the Lab Test with the same duration, similar test scope and difficulty level as before COVID outbreak. Discussion and collaboration of the Conceive and Design stage of the module project in term 1 was shifted from face to face to online.

With further combined hands-on practical in AY2021 term 2, students were adequately prepared for the module CDIO project.

To help students cope with the module in COVID scenario, then module specialist prepared more than 10 byte-sized videos for practical activities, not only with recorded practical demonstration, but also with detailed explanation of the circuit design and walk through of the source code. Module TEs assisted in part of the byte-sized practical videos preparation. While the first half of the class students were having combined hands-on practical activities face to face on campus, the 2nd half were watching the recorded practical video for the same combined hands-on activities at home, which made it smooth when it was the turn for the 2nd half class students carrying out face to face combined practicals in the Lab venue on campus in term 2.

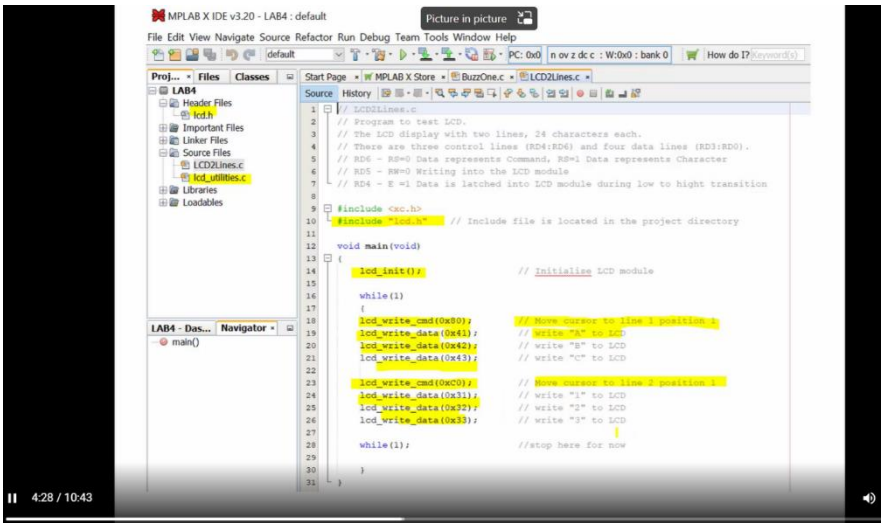
The rest part of the section presents the screenshots of examples of recorded byte-sized video for practical with circuit design explanation, source code walk through and demonstration on the in-house developed module microcontroller hardware Lab Kits.

Figure 1: Screenshot of byte-sized circuit design explanation video



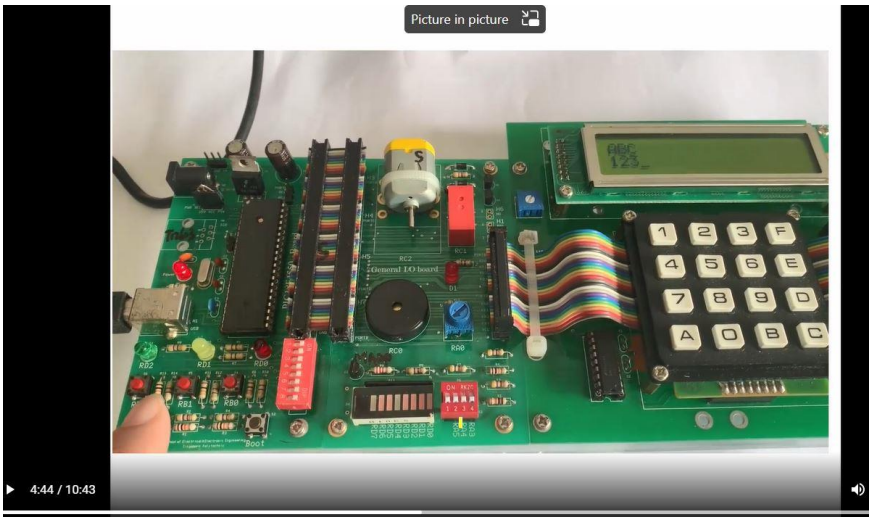
Source: MAPP module teaching and learning material

Figure 2: Screenshot of byte-sized source code walk through video



Source: MAPP module teaching and learning material

Figure 3: Screenshot of byte-sized practical demo video



Source: MAPP module teaching and learning material

To help students gain back the lost hands-on time in term 1, module TEs pre-packed microcontroller main board and components needed for module CDIO project. During June term break, each module project group took home the pre-packed hardware, while this was normally done in term 2 before COVID outbreak. In this case, students could re-practice the term 1 hands-on practical to strengthen their practical skill and / or start their CDIO project implementation earlier in the June school vacation at home, before term 2 started.

Preliminary Analysis of the Students Result of Module Assessment Components

Table 4 compares the MAPP main assessment components result of two COVID hit semesters of AY2021.

Table 4. COVID hit semesters main assessment components result

COVID Hit Semester / Passing Rate of Main Assessment Components	AY2021 S1	AY2021 S2
Lab Test	86.8%	95.4%
Mid Semester Tests	78.3%	85.1%
Project Conceive and Design	99.7%	100%
Project Implementation and Demonstration	99%	99.1%

Source: MAPP module students assessment result AY2021 S1 and AY2021 semester 2

The above table showed that for both COVID hit semesters of AY2021, the main assessment components' results were satisfactory, with the revised design-implement experiences and adjusted engineering learning workspaces in MAPP module.

The AY2021 S2 result was better than AY2021 S1 result. One reason was that throughout AY2021 S2 full semester, students had regular combined face to face hands-on practical activities, albeit bi-weekly; While in AY2021 S1 term 1, there was only e-practicals due to the outbreak of COVID. Only in AY2021 S1 term 2, the bi-weekly combined face to face hands-on practical activities could be carried out on campus with the improved COVID situation. Another reason was that after one semester learning experience in COVID scenario, the students were more ready for the learning in revised design-Implement experiences and adjusted engineering learning workspaces.

Despite only half class students having face to face combined hands-on practical on campus in the improved Covid situation, students could still produce good quality CDIO project. Based on the feedback from teaching staff and TE, the semester based module Design Contest resumed in AY2021 S2 after pause in AY2021 S1. Some winning project were Covid related, like Contactless Lift Button, etc.

Conclusion

The teaching practice presented in this paper showed that with the revised Design-Implement Experiences and Adjusted Engineering Learning Workspaces, students were able to make a rapid adaptation and transition from normal classes to online learning spaces and time-compressed face to face design – implement experience, and coped with engineering module with hands-on activities and CDIO project well.

The COVID pandemic will change the future of work and students' employability and careers.

The SDL, team working, online collaboration and mixed online with face to face collaboration experience gained from the adjustment of CDIO implementation in MAPP will benefit students in their further study and future work.

Acknowledgement

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